



SANYO Semiconductors

DATA SHEET

CMOS LSI

LC7942ND — Dot-matrix LCD Driver

Overview

The LC7942ND is a common driver LSI for driving large, dot-matrix LCD displays. It features a built-in 64-bit bidirectional shift register and a 4-level LCD driver. It can also be connected in cascade to increase the number of bits.

The LC7942ND is designed to be used with LC7940ND (QFP100) or LC7941ND (QFP100) segment drivers to drive large LCD panels.

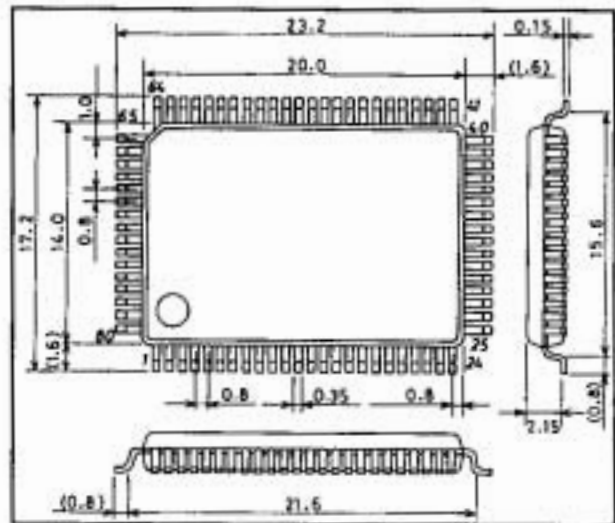
Features

- 64 built-in LCD display drive circuits
- 1/64 to 1/128 display duty cycle
- Input/outputs for cascade connection
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature
 - 5 V \pm 10% logic supply (V_{DD}) at $T_a = -20$ to $+85$ °C
 - 8 to 20 V LCD supply ($V_{DD} - V_{EX}$) at $T_a = -20$ to $+85$ °C
- CMOS process
- 80-pin flat plastic package

Package Dimensions

Unit: mm

3177-QFP80D



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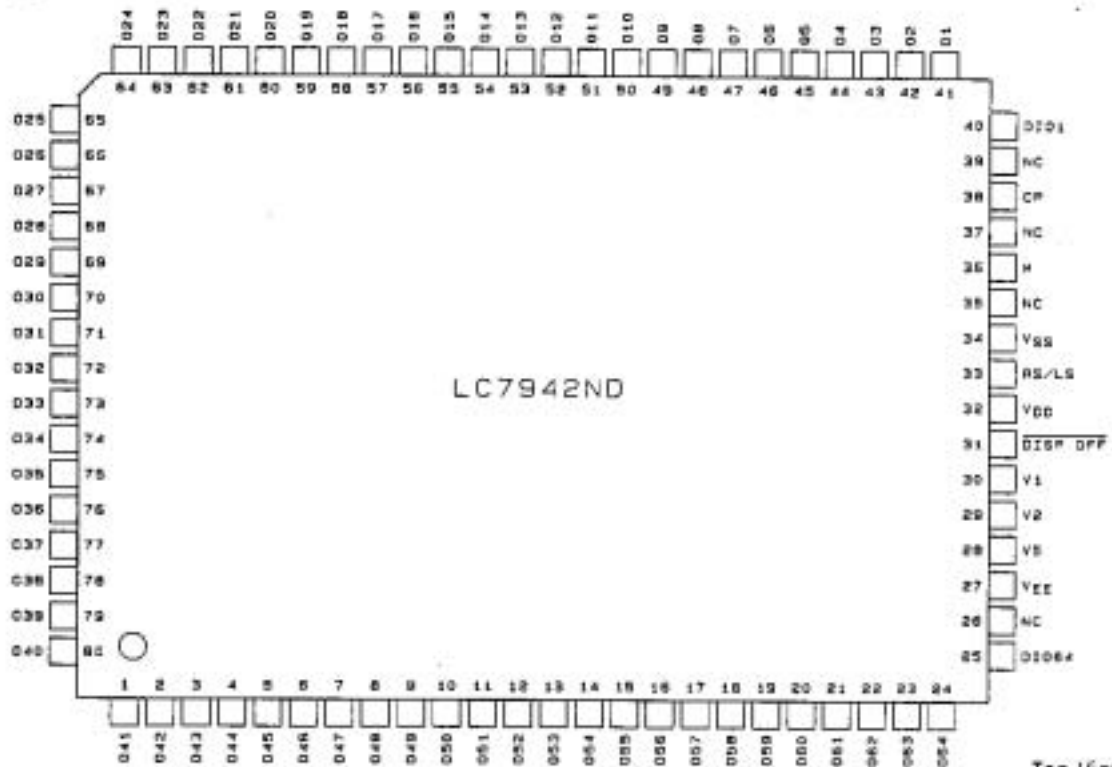
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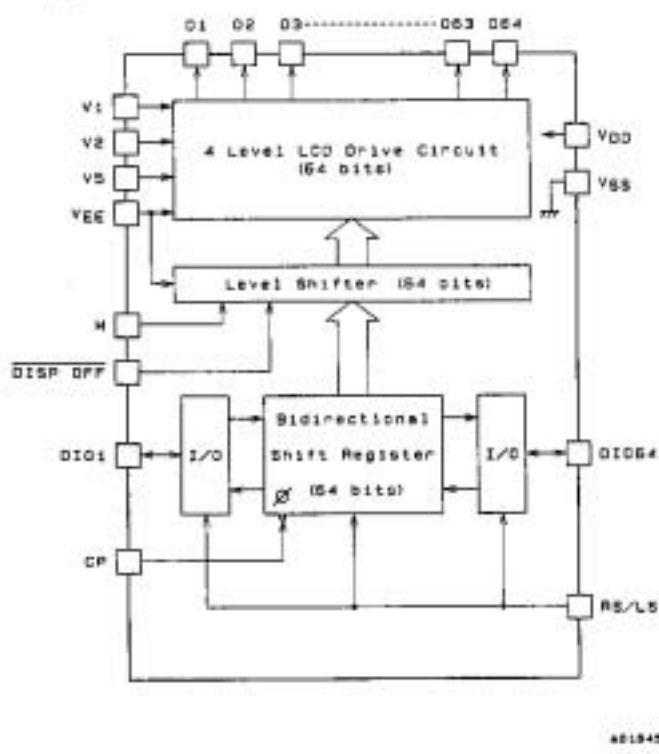
LC7942ND

Pin Assignment



Top View
A01048

Block Diagram



A01045

Pin Functions

Number	Name	IO	Function																								
32	VDD	Supply	VDD - VSS is the logic supply. VDD - VEE is the LCD supply.																								
34	VSS																										
27	VEE																										
30	V1	Supply	LCD panel drive voltage supplies. V1 and VEE are selected levels. V2 and V5 are not-selected levels.																								
29	V2																										
28	V5																										
38	CP	I	Display data input clock (falling-edge trigger).																								
40	DIO1	IO	<table border="1"> <thead> <tr> <th>RS/LS</th> <th>DIO1</th> <th>DIO64</th> <th>Shift direction</th> </tr> </thead> <tbody> <tr> <td>LOW (right shift)</td> <td>Input</td> <td>Output</td> <td>O1 → O64</td> </tr> <tr> <td>HIGH (left shift)</td> <td>Output</td> <td>Input</td> <td>O64 → O1</td> </tr> </tbody> </table>	RS/LS	DIO1	DIO64	Shift direction	LOW (right shift)	Input	Output	O1 → O64	HIGH (left shift)	Output	Input	O64 → O1												
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25	DIO64	IO																									
33	RS/LS	I																									
36	M	I	LCD panel drive voltage output alternation control signal.																								
31	DISP OFF	I	O1 to O64 output control input pins.																								
41 to 80	O1 to O64	O	LCD drive outputs. The output drive level is determined by the display data, M signal and DISP OFF input as shown below. <table border="1"> <thead> <tr> <th>M</th> <th>Q</th> <th>DISP OFF</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>HIGH</td> <td>V2</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>HIGH</td> <td>VEE</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>HIGH</td> <td>V5</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>HIGH</td> <td>V1</td> </tr> <tr> <td>x</td> <td>x</td> <td>LOW</td> <td>V1</td> </tr> </tbody> </table>	M	Q	DISP OFF	Output	LOW	LOW	HIGH	V2	LOW	HIGH	HIGH	VEE	HIGH	LOW	HIGH	V5	HIGH	HIGH	HIGH	V1	x	x	LOW	V1
M	Q			DISP OFF	Output																						
LOW	LOW			HIGH	V2																						
LOW	HIGH			HIGH	VEE																						
HIGH	LOW			HIGH	V5																						
HIGH	HIGH			HIGH	V1																						
x	x	LOW	V1																								
1 to 24	O41 to O64																										
26	NC	-	No connection.																								
35	NC																										
37	NC																										
39	NC																										

Specifications

Absolute Maximum Ratings

 $T_a = 25 \pm 2 \text{ } ^\circ\text{C}$, $V_{SS} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD max	-0.3 to +7.0	V
LCD supply voltage. See note.	VDD - VEE max	0 to 22	V
Input voltage	V1 max	-0.3 to VDD + 0.3	V
Operating temperature range	Topr	-20 to +85	°C
Storage temperature range	Tstg	-40 to +125	°C

Note

 $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$

Allowable Operating Ranges

 $T_a = -20$ to $+85$ °C, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic supply voltage	V_{DD}		4.5	–	5.5	V
LCD supply voltage	$V_{DD} - V_{EE}$	See notes 1 and 2.	8	–	20	V
DIO1, DIO64, CP, M, RSLS and DISPOFF HIGH-level input voltage	V_{IH}		$0.8V_{DD}$	–	–	V
DIO1, DIO64, CP, M, RSLS and DISPOFF LOW-level input voltage	V_{IL}		–	–	$0.2V_{DD}$	V
CP shift clock frequency	f_{CP}		–	–	1	MHz
CP pulsewidth	t_{WC}		125	–	–	ns
DIO1 and DIO64 to CP setup time	t_{SETUP}		100	–	–	ns
DIO1 and DIO64 to CP hold time	t_{HOLD}		100	–	–	ns
CP rise time	t_R		–	–	50	ns
CP fall time	t_F		–	–	50	ns

Notes

- $V_{DD} \geq V_1 > V_2 > V_3 > V_{SS}$
- At turn ON, the LCD supply should be energized after or simultaneously with the logic supply. At turn OFF, the logic supply should be cut after or simultaneously with the LCD supply.

Electrical Characteristics

 $T_a = 25 \pm 2$ °C, $V_{SS} = 0$ V, $V_{DD} = 5$ V $\pm 10\%$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DIO1, DIO64, CP, M, RSLS and DISPOFF HIGH-level input current	I_{IH}	$V_{IH} = V_{DD}$	–	–	1	μ A
DIO1, DIO64, CP, M, RSLS and DISPOFF LOW-level input current	I_{IL}	$V_{IL} = V_{SS}$	–1	–	–	μ A
DIO1 and DIO64 HIGH-level output voltage	V_{OH}	$I_{OH} = -400$ μ A	$V_{DD} - 0.4$	–	–	V
DIO1 and DIO64 LOW-level output voltage	V_{OL}	$I_{OL} = 400$ μ A	–	–	0.4	V
O1 to O64 driver ON resistance	R_{ON}	$V_{DD} - V_{EE} = 18$ V, $ V_{DE} - V_{OL} = 0.25$ V, $V_{DD} = 4.5$ V	–	–	1.5	k Ω
VDD static supply current	I_{DD}	$V_{DD} - V_{EE} = 18$ V, CP = V_{DD}	–	–	100	μ A
CP input capacitance	C_i	$f_{CP} = 1$ MHz	–	5	–	pF

Note

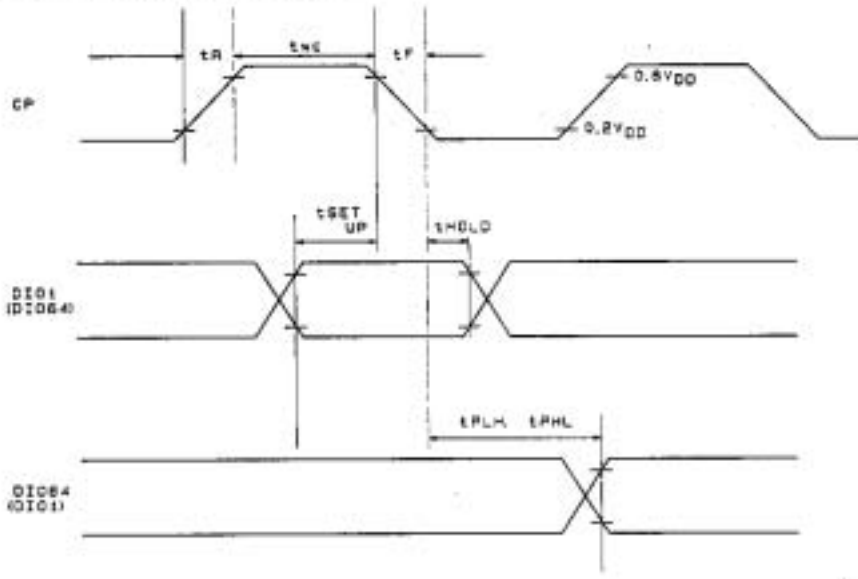
 $V_{DE} = V_1$ or V_2 or V_3 or V_{SS} , $V_1 = V_{DD}$, $V_2 = 10/11 \times (V_{DD} - V_{SS})$, $V_3 = 1/11 \times (V_{DD} - V_{SS})$

Switching Characteristics

$T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $V_{SS} = 0 \text{ V}$, $V_{DD} = 5 \text{ V} \pm 10\%$

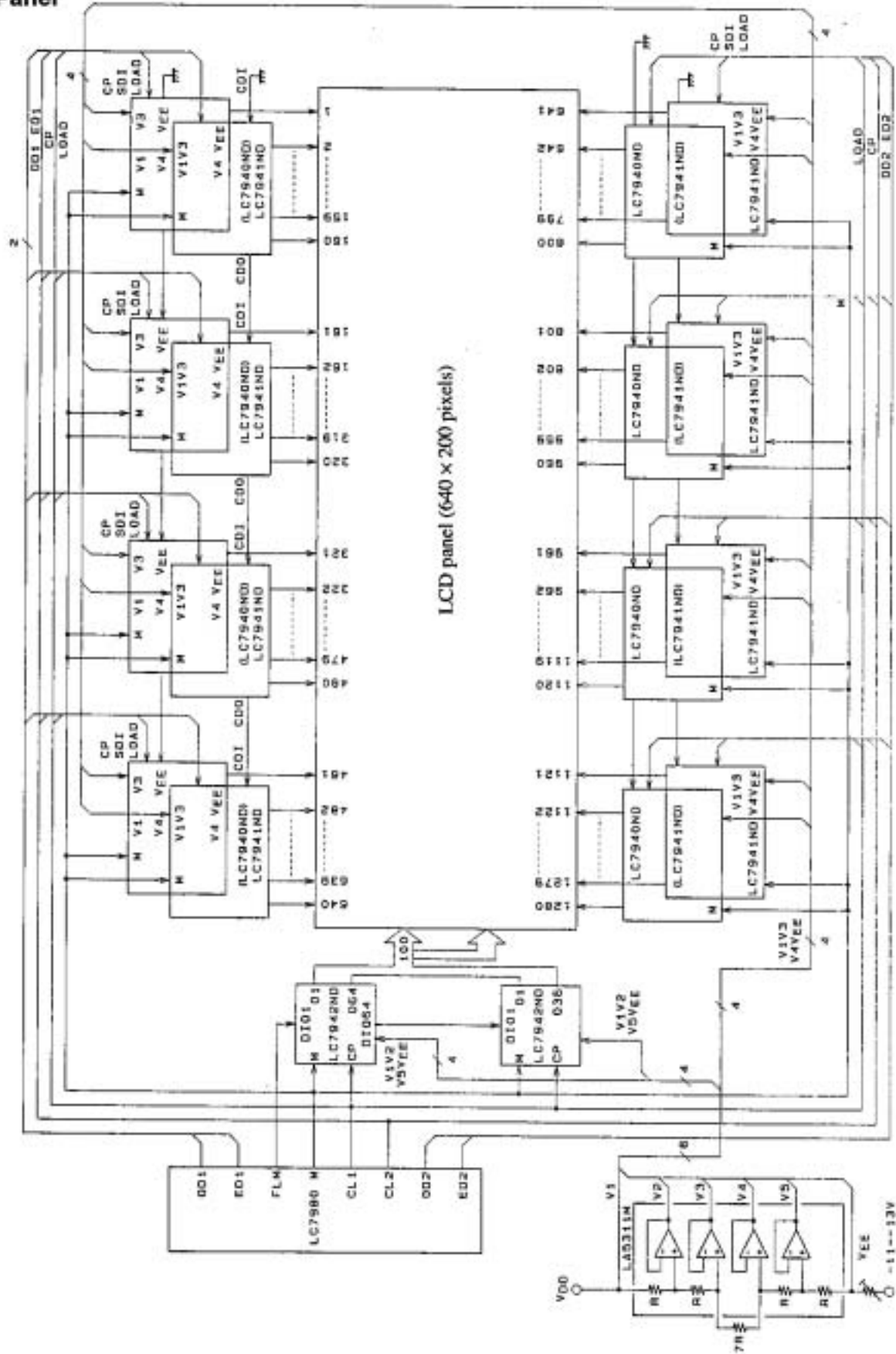
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_{PH}	$C_L = 30 \text{ pF}$	-	-	250	ns
	t_{PL}		-	-	250	

Switching Characteristics Waveform



AD1048

LCD Panel



AS1847